REMARKS

Claims 77–96 are pending in the present application.

Claim 81 was amended to correct a typographic error.

Claims 87–96 were added.

Examination of the application on the merits is respectfully requested.

35 U.S.C. § 103 (Obviousness)

Claims 77–86 were rejected in the parent application under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,422,289 to *Pierce et al* in view of U.S. Patent No. 5,346,587 to *Doan et al*. This rejection is respectfully traversed.

Independent claim 77 recites that the source and drain regions each include a first portion in the substrate and a second portion on the substrate over the first portion and adjacent to the insulating material on the sides of the gate electrode. Such a feature is not shown or suggested by the cited references.

The Office Action states:

> Applicant argues that Pierce fails to show a second portion of the source/drain above the substrate. However, the examiner does not understand the difference structurally between the invention of Pierce and applicant as claimed. Furthermore, in the abstract, Pierce refers to source and drain 38 and 40 as "source and drain areas". For example, column 11, lines 29–46 talk about forming regions 38 and 40 using epitaxial growth to form single-crystal or polysilicon regions.

Paper No. 13, page 2. As is known in the art, MOSFET source and drain regions are the portions of the transistor in which charge carrier generation and recombination occur for the charge carriers which form the current. Saturation current, and therefore transconductance, of the transistor may be constrained by the size of the source drain regions. Additionally, depletion regions around the source and drain isolate those regions from the body of the substrate.

Pierce et al discloses in Figure 5 a structure in which the source and drain regions 34 and 36 are completely within the substrate:

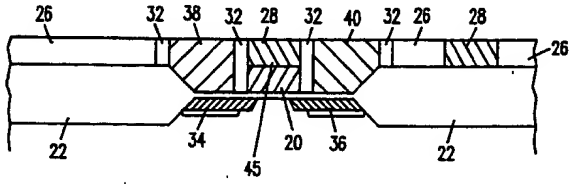

FIG. 5

Conductive contacts or plugs 38 and 40 over the source and drain regions 34 and 36 are merely conductive structures for electrically contacting source and drain regions 34 and 36, not a part of source/drain regions 34 and 36, and therefore do not satisfy the claim limitation of "a second portion." The structural difference between the claimed invention and the structure shown in *Pierce et al* is that the semiconductor material over the substrate forms source and drain regions in the claimed invention, while plugs 38 and 40 are merely electrical contacts to source/drain regions 34 and 36 in *Pierce et al*. This structural difference is especially clear in light of newly

added claims 88, 93 and 96, which recite that the dopant concentration within the raised source/drain regions is suitable for heavily doped source drain regions. Such a feature is not shown or suggested by *Pierce et al*, which suggests that plugs 38 and 40 maybe doped but does not specify any doping level. In fact, *Pierce et al* teaches away from this limitation in that the conductive plugs 38 and 40 must be heavily doped to form good conductor, a low resistance electrical contact to the source and drain regions.

Pierce et al contains no teaching or suggestion that plugs 38 and 40 are or could be modified to form part of the source/drain regions for the transistor. Moreover, *Pierce et al* teaches that conductive plugs 38 and 40 may be metallic, teaching away from employing raised source/drain regions over the substrate as claimed. *Pierce et al* teaches formation of the transistor structure entirely within the substrate in accordance with the conventional art, with conductive plugs filling the contact openings to planarize the structure. In contrast, the present invention forms a portion of the source/drain regions above the substrate, effectively wrapping the transistor structure around the edges of the gate electrode, allowing a smaller total lateral size for the transistor. *Pierce et al* does not teach or suggest forming the source and drain regions in two portions within and over the substrate.

Therefore, the rejection of claim 77–86 under 35 U.S.C. § 103 has been overcome.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claim 81 was amended herein as follows:

81. (amended) The integrated circuit structure of claim 77, further comprising:

LDD regions for the source and drain regions formed within the first portion of each source and drain region.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@novakov.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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